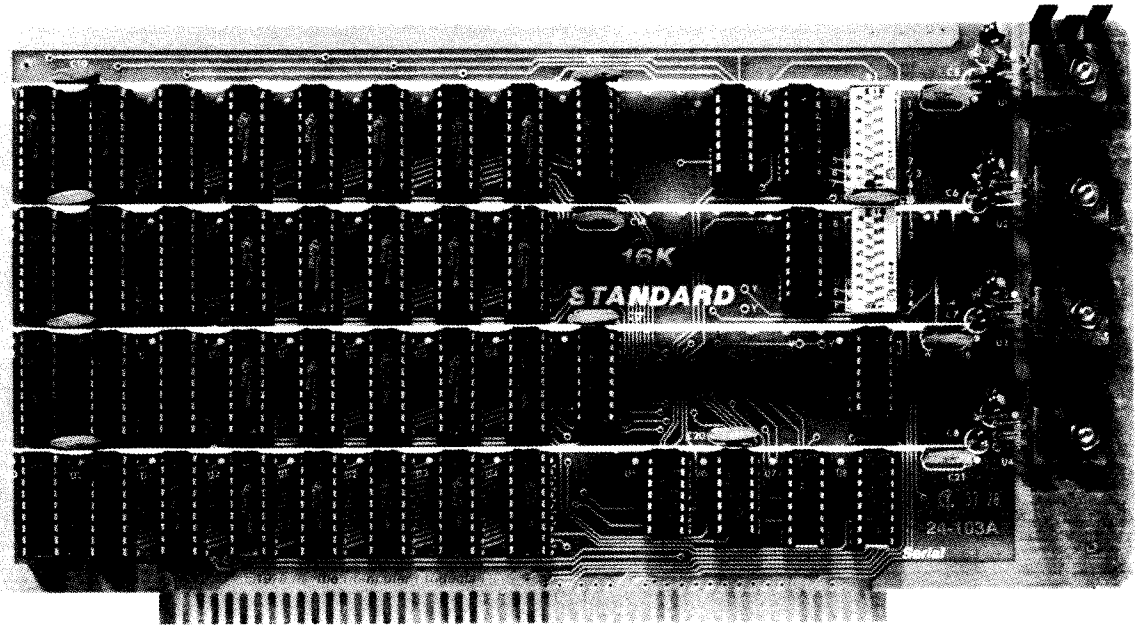
Instruction Manual

Model 24-103



16K STANDARD

S-100 Bus Static RAM

Your Model 24-103 16K STANDARD RAM was designed to provide you with a cost effective, reliable product which would operate without difficulty in the vast majority of S-100 Bus systems now on the market.

It incorporates state-of-the-art features such as Schmitt trigger inputs on all data and control lines to the board and uses LSTTL buffering for address inputs A-0 through A-11. It uses DIP switches for easy address changing and also provides the capability of being "parallel addressed".

BOARD REVISION B
MAN103 - 3-5-80

Seattle Computer Products, Inc.
1114 Industry Drive, Seattle, WA. 98188
(206) 575-1830

1.0 CONFIGURING THE BOARD

No action other than setting the addresses is required to make your 16K STANDARD RAM interface with nearly all of the S-100 systems now being sold. Listed below are some of the systems which may require special consideration.

CROMEMCO Z2D, ETC.

For operation in the lowest 48K of memory space:

1. Set addresses of board on S-1 and S-2.

The board is not designed to operate in the highest 16K of address space in a Cromemco system or in systems using bank select. See our PLUS and APEX boards for use in this situation.

ALPHA MICRO

For operation in the lowest 60K of address space:

1. Set addresses of board on S-1 and S-2.

2. Change "V" jumper from "1" to "2". The jumper is located just to the left of U52.

With this jumper changed, up to 60K of 16K STANDARD RAM boards may be used in an Alpha Micro system. Typically, they will be addressed as follows:

Board	Address Switches "on"
1	0, 1, 2, 3
2	4, 5, 6, 7
3	8, 9, A, B
4	C, D, E

(Note that only 12K is used on board 4)

OTHER SYSTEMS

If your board does not function correctly immediately, try changing the "V" jumper. This changes the "write" signal from MWRITE to PWR*. If the board still fails to function correctly, it will be necessary for you to read section 3.0 of this manual (page 5) which describes the board configuration jumpers. Help is also available from the factory.

* This symbol indicates the signal (PWR, in this case) is active low.

2.0 RAM BOARD ADDRESSING

MEMORY SLOTS

The numbers (0 through F) on the left side of the two DIP switches represent the 16 possible 4K "slots" which most CPUs are capable of directly addressing.

MEMORY BLOCKS

The numbers (1 through 4) on the right side of the two DIP switches represent the four "blocks" into which the memory board has been divided. Each block is 4K in size.

Upon examination of the board, it will be seen that each "block" can be connected to four possible 4K slots. For example: block 1 can be connected (by throwing the DIP switch segment opposite it to the "on" position) to memory slots 0, 4, 8, and C. Block 2 can be connected to the memory slots 1, 5, 9, and D, etc.

NORMAL ADDRESS SELECTION

Normally, four successive memory slots will be selected for the board. As an example: selection of the lowest 16K of address space for this board is accomplished by throwing the switch segments opposite slots 0, 1, 2, and 3 to the "on" position. Selecting the next 16K would be accomplished by throwing the switch segments opposite slots 4, 5, 6, and 7. Higher addresses would be selected in a similar manner.

Note that in all of these "normal" address selection cases, each "block" is addressed by ONE AND ONLY ONE memory slot address.

PARALLEL ADDRESSING

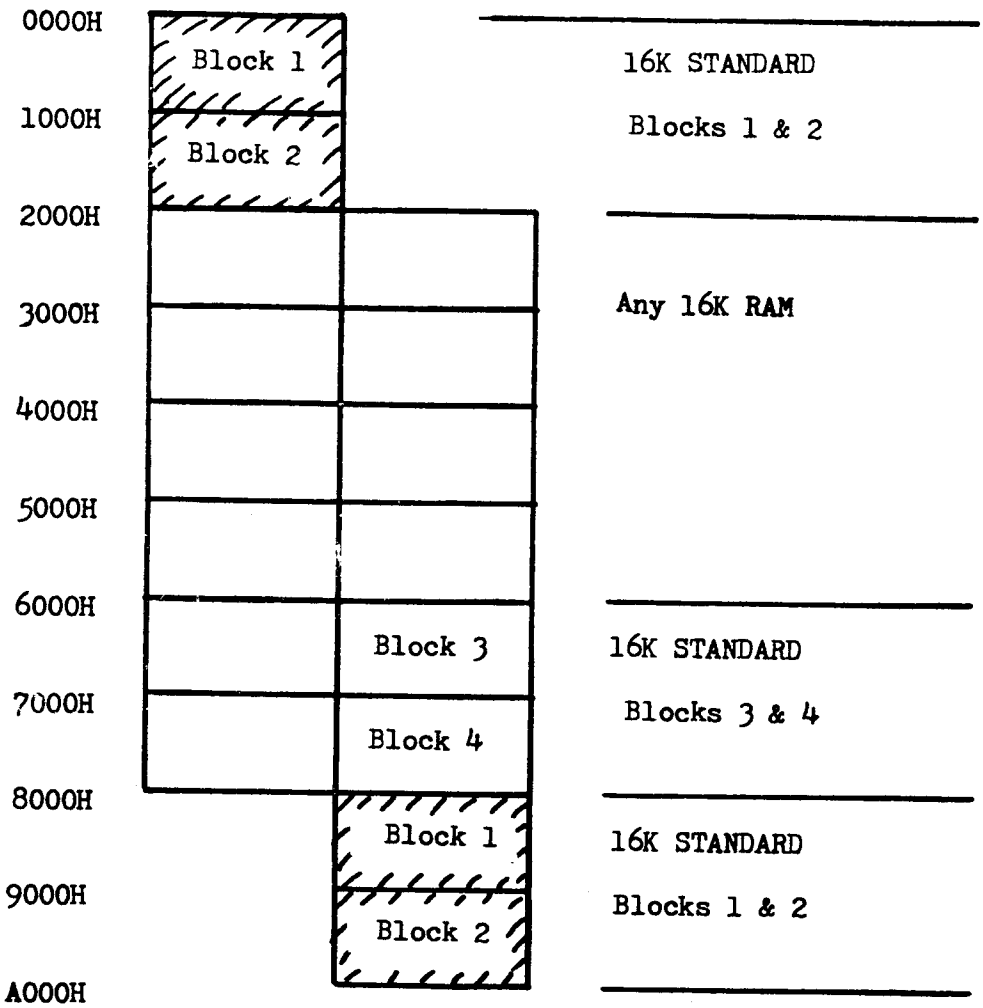
Parallel addressing allows you to have your RAM located at one address for one type of software and at another address for another type of software. This feature helps take care of the problem you run into when your software has different starting addresses.

An example may help illustrate this situation. North Star software begins at 2000H. Perhaps your "game package" begins at 0000H. Do you "waste" the lowest 8K while running North Star BASIC?

There are several solutions. One, you can buy 64K of memory and forget the problem. Two, you can physically "relocate" RAM whenever you switch software. Or, three, you can use "parallel addressing".

The memory map on the next page illustrates how parallel addressing may be used to make 32K of RAM look like 40K to your computer. Two 4K blocks of RAM are parallel addressed at both 0000H through 1FFFH and 8000H through 9FFFH.

For software beginning at 0000H, you have 32K running from 0000H to 7FFFH. For software originating at 2000H, you have 32K running from 2000H through 9FFFH. You can switch RAM "one the fly" without any physical change to the board. The two 4K blocks which are parallel addressed are shown cross hatched on the figure. Other parallel addressing schemes will also work.



3.0 BOARD CONFIGURATION JUMPERS

There are three jumpers on the board which will allow you to "customize" it to your specific system. In most cases changing these jumpers will not be required unless you have a "non-standard" type system. This section describes these jumpers and the effect of changing them.

SOUT OPTION

Most systems use the SOUT signal. The purpose of the signal is to disable RAM while the system CPU is "outputting" data to a peripheral which has the same address as system RAM. A "high" on the SOUT line tells the RAM in the system to ignore the output instruction.

If your system does not use SOUT, cut the trace between jumper pads "W - W", located just to the right of U52.

MWRITE / PWR* OPTION

A few systems do not generate MWRITE. If your system is one which does not generate this signal, it will be necessary to use PWR* to control writing into your RAM board. To make this alteration, change the "V" jumper from position "1" to position "2". The "V" jumper is located just to the left of U52.

PHANTOM* OPTION

Some Processor Technology (and other) systems use bus line 67 for a PHANTOM* signal which disables RAM while a ROM, co-located in the same address space, is being read. If your system uses this signal, jumper between pads "Y - Y", located just to the right of the word "STANDARD" on the board.

4.0 THEORY OF OPERATION

The key to understanding the operation of the 16K STANDARD RAM board circuitry is to consider it a "memory array" with supporting circuits to buffer inputs and outputs and control circuits for determining when a read or a write operation is desired.

It is suggested you follow along on the schematic (page 10) while reading this section of the manual.

MEMORY ARRAY

The memory array includes 32 4K by 1 static RAM chips (4044 type) organized into four blocks of 4K by 8 each. All address changes and write commands are fed to all 32 chips; however, only the eight chips "selected" by the low chip select signal will be active.

Data to the board, (CPU Data Out Bus) is also continually being sent to all 32 chips. However, to "write" new data into the chips requires several actions including a low CS signal to the particular block and a write command. The output buffers on the chips are in the "high impedance state" unless the chip is selected by the low CS signal.

Note the identification of the chips: U11 is block 1, bit 1; U12 is block 1, bit 2; etc. In general, the first digit of the IC number in the memory array designates the "block" while the second designates the bit postion.

ADDRESS BUFFERS

Address lines A-0 through A-11 are buffered by 74LS368 buffers. These buffers provide low loading to the system bus. They are capable of high current output for fast switching of address information in the memory array. These buffers are enabled at all times so address information at the chips continuously follows the bus.

BLOCK SELECT

The block select circuity accepts addresses A-12 through A-15 as well as SOUT as inputs. It decodes these inputs to determine if this particular RAM board is being addressed.

Assuming SOUT is low, the block select circuity decodes the A-11 through A-15 to obtain a unique low signal on one of the sixteen outputs of the two 74LS156 decoders. If this "low" signal corresponds to a switch segment of S-1 or S-2 which is "closed", the chip select line connected to the switch will be pulled low, enabling that block of RAM in the memory array.

Note for addressing purposes that each chip select line will respond to only four 4K slots out of the sixteen available. For example, chip select line CS1* will respond to addresses 0xxxH, 4xxxH, 8xxxH, and CxxxH only.

Normal addressing procedure is to connect each 4K RAM block to only one of the 16 possible "memory slots". If more than one is connected, the block of RAM will respond to more than one address. This is called "parallel addressing". Parallel addressing offers the system user certain advantages which were discussed on page 4.

MEMORY WRITE

Data can be written into your RAM board using one of two possible control paths. As shipped from the factory, MWRITE is the signal used. For a memory write to occur in this configuration, one of the chip select lines must be low and the MWRITE signal must be high.

For the systems which do not generate MWRITE, PWR* may be selected as the write control signal. With this selection, both the chip select line and the PWR* line must be low to cause a write into memory to occur. The MWRITE / PWR* option is selected by the "V" jumper. In position "1", MWRITE is selected. In position "2", PWR* is selected.

DATA OUT BUFFERS

The data out buffers are U7 and U8, both 74LS368s. They provide high driving current to the bus. The buffers will source 2.6 ma. and sink 24 ma. and should operate without difficulty in all systems including those with bus terminators. The data out buffers are controlled by the data out buffer control circuit.

DATA OUT BUFFER CONTROL

The data out buffer control circuit consists of half of U53 and its inputs. If this particular board is addressed, the output on pin 8 of U53 goes high enabling the remainder of the circuit. If both SMEMR and PDBIN go high, the data out buffer enable signal (pin 6 of U53) will go low, enabling the data out buffers.

DATA IN BUFFERS

The data in buffers are contained in U5 and U6, both 74LS14s. These chips provide low loading on the bus lines and have hysteresis inputs (Schmitt trigger) for high noise immunity.

POWER SYSTEM

The power system consist of four nearly identical circuits. Considering the one containing U1, C1 prevents oscillations of the regulator circuit. C5, C10, C11, and C12 provide transient suppression on the +5 volt line. Bus bars are used for this design. They provide a very low impedance power distribution line and greatly reduce voltage transients on the line. The regulator provides both overcurrent and thermal shutdown in the event of a fault on the +5 volt line.

5.0 REPAIR SERVICE

Repair service is available at the factory for any product manufactured by Seattle Computer Products. For items under warranty, there is no charge for this service. For repair of boards which are no longer under warranty coverage, return the board to the factory at the address shown below. If the board can be repaired for no more that $25 we will go ahead with the repair and ship the repaired board to you COD for the amount of the repair. If the cost will exceed $25, we will notify you before we begin work. Most memory board repairs are in the $15 to $20 cost range. Include your telephone number with returned boards.

Normal factory repair time is 48 to 72 hours.

Ship all returned boards to:

Seattle Computer Products
1114 Industry Drive
Seattle, WA 98188
(206) 575-1830

6.0 SPECIFICATIONS - MODEL 24-103 16K STANDARD RAM

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP*	MAX	UNITS
Power Supply Voltage	7.5		13.5	volts
Power Supply Current		1.5		amps
High Level Signal Input	2.0		5.5	volts
Low Level Signal Input	-0.5		0.8	volts
High Level Input Current			20	uamps
Low Level Input Current			400	uamps
Hysteresis				
A-0 - A-11		0		volts
All Others	0.4	0.8		volts
Data Out Voltage				
High Level - 2.6 ma. source	2.4	3.1		volts
Low Level - 24 ma. sink		0.35	0.5	volts
High-Z Current	-20		+20	uamps

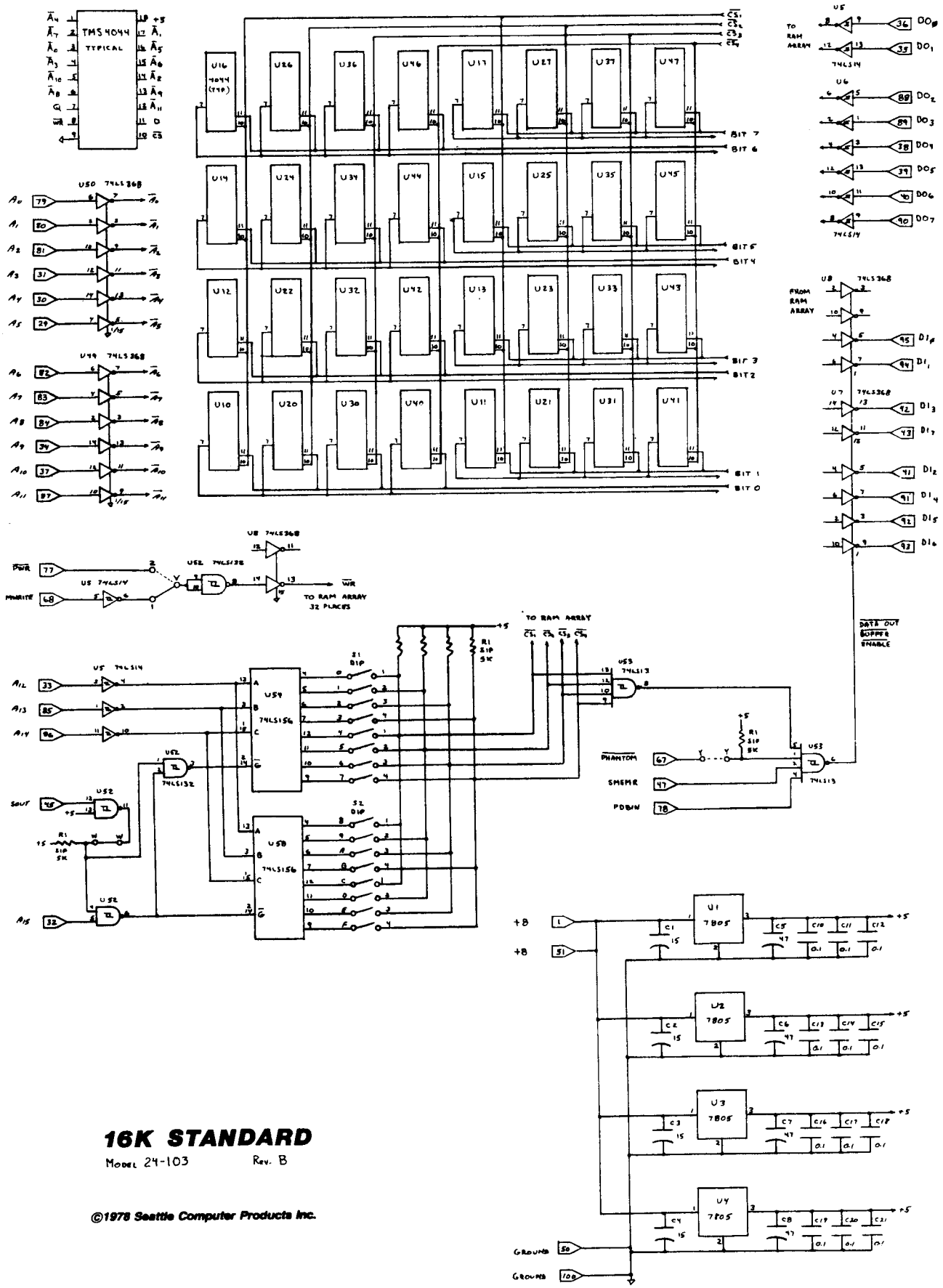
AC CHARACTERISTICS

CHIP SPEED	200	250	300	nsec.
Access and read times	236	286	336	nsec.
Write cycle time	218	268	318	nsec.

THERMAL CHARACTERISTICS

Operating environment 5 to 65 degrees Centegrade

* TYP is 25 degrees Centigrade.



16K STANDARD

Model 24-103 Rev. B

One-Year Limited Warranty

WARRANTEE AND WARRANTY PERIOD

The Seattle Computer Products (hereinafter referred to as SCP) warranty for this product extends to the original purchaser and all subsequent owners of the product for a period of one year from the time the product is first sold at retail and for such additional time as the product may be out of the owner's possession for the purpose of receiving warranty service at the factory.

WARRANTY COVERAGE

This product is warranted to be free from defects of material and workmanship and to perform within its specifications as detailed in the instruction or operating manual during the period of the warranty.

This warranty does not cover damage and is void if the product has been damaged by neglect, accident, unreasonable use, improper repair, or other causes not arising out of defects in material or workmanship.

WARRANTY PERFORMANCE

During the warranty period, SCP will repair or replace defective boards or products or components of boards or products upon written notice that a defect exists. Certain high value parts may have to be returned to SCP prior to replacement. Other components will be replaced without the part having to be returned to the factory with the exception the SCP retains the right in all cases to examine the defective board or other products prior to the items replacement under the warranty. In the event the return of the board, product, or component is requested by SCP under this warranty, the owner shall ship the item prepaid to the SCP factory. SCP will pay for shipment of replacement items back to the owner. All repairs or replacements under this warranty will be performed by SCP within five working days of receipt of notice of defect or return of components as called for under this warranty.

WARRANTY DISCLAIMERS

While high reliability was a major design factor for this product and care was used in its manufacture, no certainty can be achieved than any particular product will operate correctly for any specific time. No representation is made by SCP that this product will not fail in normal use. Because of the inability to guarantee 100% reliability, SCP shall not be liable for any consequential damange the user may suffer because the products fails to function reliably 100% of the time. Any implied warranties arising from the sale of this product are limited in duration to the warranty period defined above.

LEGAL REMEDIES

This warranty gives the purchaser specific legal rights. He may have additional rights which vary from state to state.

SHIPPING INSTRUCTIONS

In the event it becomes necessary toreturn the product or component to SCP, also return a written explaination of the difficulty encountered along with your name, address and phone number. Package the items in a crushproof container with adequate packing material to prevent damage and ship prepaid to:

Seattle Computer Products
1114 Industry Drive
Seattle, Washington 98188